HIGH SPEED INTERFACING WITH FPD-LINK DISPLAYS

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Introduction

FPD-Link is an open standard developed by National Semiconductor widely used as a digital interface for LCD panels from the late 90s until the mid 2010s. Having been phased out in favor of eDP in recent years, many LCD displays utilizing this standard have reached their End Of Life and are left unused. These displays can reach resolutions in excess of 1920×1200 at a refresh rate of 60 Hz, and are typically very thin and lightweight, making them attractive for re-use in projects.

Aims & Objectives

This project aims to interface FPD-Link displays using an FPGA, accepting a parallel video interface as an input source, such that of a GameBoy Advance. The FPGA of choice is the Altera Cyclone IV E and the display is a 1024×600 pixel LCD panel with a refresh rate between 55 and 65 Hz.[1]

FPD-Link Data Framing

For an 18-bit-per-pixel display, the required video signals consist of 6 bits of color depth per color, horizontal sync, vertical sync, and display enable. These are serialized at a ratio of 7:1, as shown in Fig. 1, meaning the serial clock is 7 times faster than the pixel clock.[2]

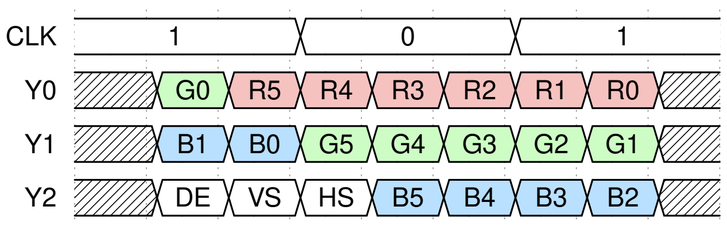

Figure 1: Data Framing

This is achieved on the Cyclone IV using Altera's ALTLVDS_TX IP core, which is seen on the right of Fig. 4. The serializer is configured to accept 21 parallel input signals and an input clock, and outputs a pixel clock and 3 serialized data channels.

Clocks

The LCD being used is a 1024×600 18-bit-per-pixel display, meaning there's 6 bits of depth per color. At 60Hz, the horizontal blanking is 176 pixels wide, and the vertical blanking is 25 pixels tall, totalling an effective resolution of 1200×625 pixels. As a result, the required pixel clock is 1200×625×60 = 45 MHz. The FPGA's onboard oscillator runs at 50 MHz, so a PLL is used to multiply the clock by 9 and divide it by 10. The serializer outputs a 45 MHz clock with a 57% duty cycle to match the 2-3-2 clock pattern shown in Fig. 1.

Fig. 2 compares the 45 MHz PLL clock to the 45 MHz serializer clock, and shows the the first pixel high in channel 1, shifted 101.25º to align with the pixel clock.

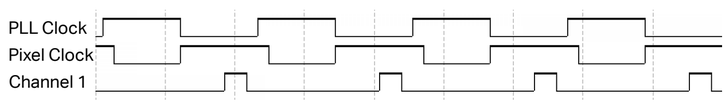

Figure 2: Clocks

Timing Signals

The VSync, HSync, and DE timing signals are derived from the PLL's clock using counters and magnitude comparators. VSync is high whenever a pixel is horizontally in the display's active area, HSync is high whenever a pixel is vertically in the display's active area, and DE is high whenever VSync and HSync are both high.

The VSync and HSync signals are created by comparing the magnitude of a counter that is incremented once per clock cycle, as in Fig. 3.

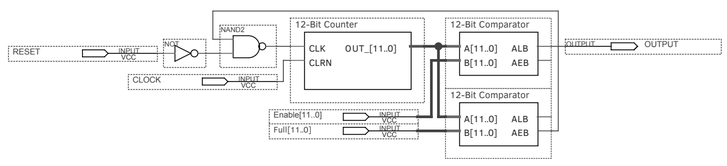

Figure 3: HSync Signal Generator

These two signals are ANDed to create the DE signal, resulting in the circuit on the left of Fig. 4.

GameBoy Advance Integration

For easy easy interfacing with the GBA's video signals, each signal was broken out to a 2.54 mm pin header:

Figure 5: DevBoy Advance

The onboard oscillator was also removed and replaced with a PLL on the FPGA, overclocking the refresh rate from 59.7 Hz to 60 Hz, therefore facilitating synchronization between devices and reducing screen tearing on the FPD-Link LCD.

Results

The main premise of this project, FPD-Link video generation on an FPGA, has been successfully and thorouglhy tested in simulations at various resolutions ranging from 10×6 to 1024×600 pixels running at 60 Hz. By implementing 12-bit counters and comparators, displays of up to 4095×4095 at arbitrary refresh rates are supported, dependant on the speed grade of the FPGA used.

There is currently preliminary support for video capture from the GBA, including circuitry to convert the GBA's RGB555 pixel data to the LCD's RGB666 color format. Given that no pixel clock is present on the GBA, it is derived from the PLL acting as the GameBoy's oscillator.

Future Work

Due to the difference in voltage of the FPGA's LVDS output and the LCD's required LVDS input, further work is needed in order for communication between both devices to occur.

Additional circuitry will be designed to adjust the aspect ratio and size of the GameBoy's video on the LCD due to mismatched resolutions.

Timing Signals Generator and Frame Serializer

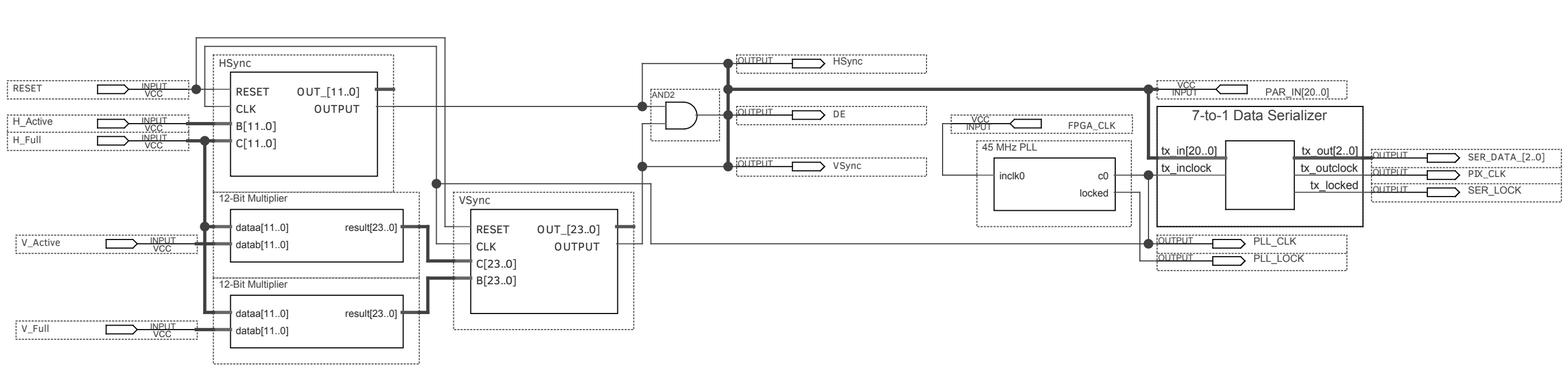

Figure 4: Circuit Overview

References

[1]: HannStar, "HSD089IFW1-A00 Product Specification", August 2008
[2]: Texas Instruments, "AN-1032 : An Introduction to FPD-Link", July 1998

All figures in this poster are the author's own.

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